MIL-M-38510/221A(USAF)
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SUPERSEDING
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MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 16,384 BIT, MOS, ULTRAVIOLET ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EPROM), MONOLITHIC SILICON

This specification is approved for use by the Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel MOS erasable programmable read-only memory microcircuits which employ the ultraviolet light erasing technique. One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be as specified in MIL-M-38510, except the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	2048 X 8-bit EPROM

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
J	D-3 (24-lead, 1/2" x 1-1/4"), dual-in-line package 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC} 2/	-0.3 V to 6.0 V
All input or output voltages 2/	-0.3 V to 6.0 V
Program input, Vpp	-0.3 V to 26.5 V
Operating case temperature range 3/	-55°C to +125°C
Storage temperature range	-65°C to +125°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	30°C/W
Maximum power dissipation, (P_D) per device	
Programming	1.88 W
Operating	1.0 W
Junction temperature (T_J)	+160°C

1/ The lid shall be transparent to permit ultraviolet light erasure.
2/ Under absolute maximum ratings, voltage values are with respect to ground, unless otherwise specified. Throughout the remainder of this data sheet, voltage values are with respect to ground.
3/ The device will be functional at 125°C. However, sustained operation above 100°C will reduce data retention time.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage V_{CC}	4.5 V dc to 5.5 V dc
Minimum high level input voltage, V_{IH}	2.0 V dc to V_{CC} +1
Maximum low level input voltage, V_{IL}	-0.1 V dc to 0.80 V dc
High level program input voltage, $V_{IH(PR)}$	24 V to 26 V
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2A.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification. The truth table for programmed devices is shown on figure 2B.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Functional tests. The functional tests used to test this device is contained in the table III notes. If the test patterns cannot be implemented due to test equipment limitations, then alternate patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.2.5 Case outline. The case outline shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.7.

3.7.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table IV.

3.7.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall consistute a device failure, and shall be removed from the lot.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 47 (see MIL-M-38510, appendix E).

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line; not necessarily the line producing the device type described herein.

3.10 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions (unless otherwise specified) 2/ T_C = -55°C to +125°C	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 2.4 V, I_{OH} = -400 µA	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 2.1 mA		0.45	V
Output leakage current	I_{LO} 3/	V_{CC} = 5.5 V, V_{OUT} = 5.5 V, $\overline{CE}$ = 2.4 V		10	µA
High-level input current	I_{IH}	Address and chip enable $\overline{CE}$: V_{CC} = 5.5 V, V_{IN} = 5.5 V		10	µA
Low-level input current	I_{IL}	Address and chip enable $\overline{CE}$: V_{CC} = 5.5 V, V_{IN} = 0.80 V		10	µA
Supply current (standby)	I_{SB} 4/	V_{CC} = 5.5 V, $\overline{CE}$ = 2.4 V, V_{IN} = 2.4 V, $\overline{OE}$ = 2.4 V, Outputs = Open		30	µA
Supply current	I_{CC} 4/	V_{CC} = 5.5 V, V_{IN} = 2.4 V, $\overline{OE}$ = $\overline{CE}$ = 0.8 V, Outputs = Open		115	mA
Program current	I_{pp} 4/	V_{pp} = 6.1 V; T_C = +25°C		5	mA
		V_{pp} = 6.1 V; T_C = +125°C and -55°C		10	mA
Propagation delay times:					
CE to programmed outputs	t_{PZH1}, t_{PZL1}	V_{CC} = 5.5 V, see figure 4, $\overline{OE}$ = V_{IL}		450	ns
Address inputs to outputs (access time)	t_{PZH2}	V_{CC} = 5.5 V, see figure 4		450	ns
	t_{PZL2}	$\overline{CE}$ = V_{IL}		450	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions (unless otherwise specified) 2/ T_C = -55°C to +125°C	Limits Min	Limits Max	Unit
Output enable to outputs	t_{PHZ3} t_{PZL3}	V_{CC} = 5.5 V, see figure 4 $\overline{CE}$ = V_{IL}		150	ns
Output enable high to output float	t_{PHZ1} t_{PLZ1}			130	ns
Address to output hold	t_{PHZ2} t_{PLZ2}	V_{CC} = 5.5 V, $\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		ns

1/ DC and read mode.

2/ See table III for exact pin test conditions.

3/ Connect all address inputs and the $\overline{CE}$ input to V_{IH} and measure I_{LO} with the output under test connected through a current meter to the voltage specified.

4/ V_{PP} may be directly connected to V_{CC} except during programming. The supply current would then be a sum of I_{CC} and Ipp.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Group B test requirements (method 5005)	N/A
Group C end-point electrical parameters (method 5005)	1,2,3,7,8
Additional electrical subgroups for group C periodic inspections	None
Group D end-point electrical parameters (method 5005)	1,2,3,7,8

Notes:
1. *PDA applies to subgroup 1 and 7 (see 4.2c).
2. Any or all subgroups may be combined when using high-speed testers.
3. Subgroups 7 and 8 shall consist of verifying the binary count pattern.
4. For all electrical tests, the device shall be programmed to the pattern specified.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883). Test condition D, or E using the circuits shown on figure 5 or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7 tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

d. A programmability test shall be performed when programming the devices for 4.2e (1) using an LTPD of 10.

e. A bit retention test shall be performed prior to burn-in and shall consist of the following:

(1) Program all devices with the complement of the binary count pattern (see 3.7.2 and 4.2d).

(2) Verify pattern (see 3.7.3).

(3) Remove all device terminal connections (including supply voltages).

(4) Perform a high temperature storage for 48 hours at 150°C.

(5) Restore device terminal connections.

(6) Verify pattern (see 3.7.3).

(7) Erase the pattern and program devices with a binary count pattern (see 3.7.2).

(8) Verify pattern (see 3.7.3).

(9) Burn-in (see 4.2a).

(10) Verify pattern (see 3.7.3) at 125°C.

f. After completion of all testing, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing).

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data may be used to satify the requirements for group C and D inspections (see 6.7).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

a. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

b. A special subgroup shall be added using an LTPD of 15 for class B. This subgroup shall consist of a high voltage test of the input protection circuits, V_{ZAP} (see 4.8).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E, using the circuit shown on figure 5, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified and reprogrammed with a binary count pattern. Any device failing the erasure-verify test shall be considered a failure. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.4.3). The devices to be submitted to the steady-state life testing shall be subjected to the following tests and inspections. Each device in the sample shall be subjected to a minimum of 50 program and erase cycles. Each cycle shall consist of the following steps.

(1) Program all devices with a binary count pattern.

(2) Verify pattern (see 3.7.3).

(3) Erase (see 3.7.1).

(4) Verify pattern (see 3.7.3).

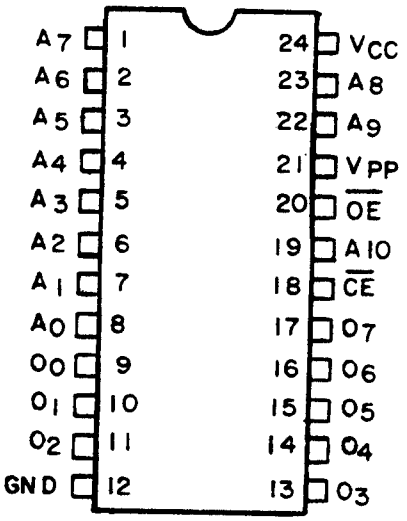


FIGURE 1. Terminal connections.

A.

Truth table (Unprogrammed) 1/

Word	Inputs			Outputs 2/
Number	$\overline{OE}$/PGM	$\overline{CE}$	$A_{10}A_9A_8A_7A_6A_5A_4A_3A_2A_1A_0$	$O_7O_6O_5O_4O_3O_2O_1O_0$
X	GND	L	← X →	H H H H H H H H
X	GND	H	← X →	← HI-Z →

B.

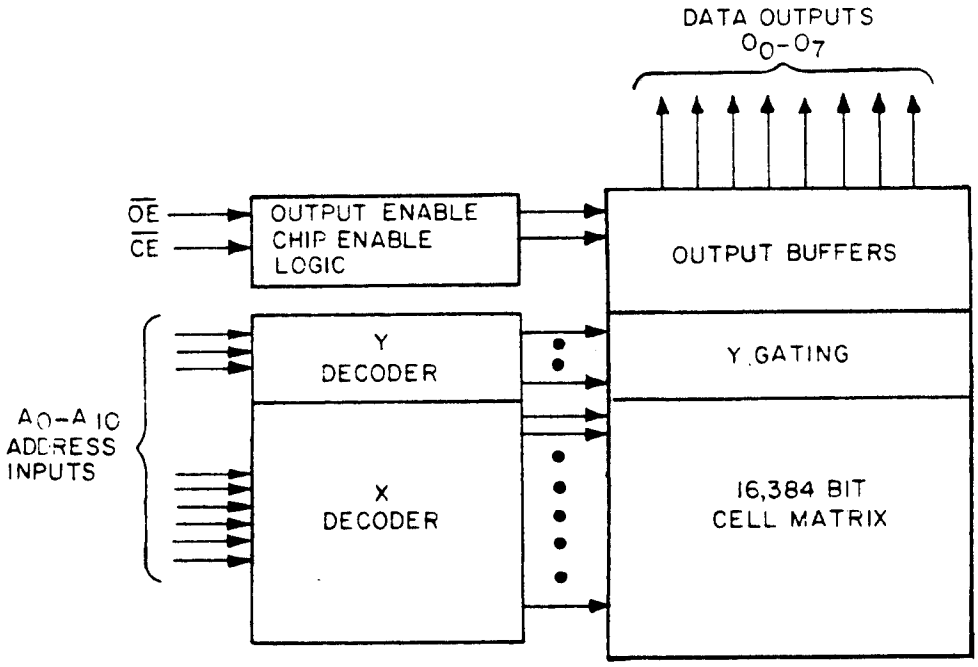
Truth table (Programmed) 1/

Mode	Input				Outputs
	$\overline{CE}$	$\overline{OE}$	$+V_{PP}$	$+V_{CC}$	
Read	L	L	5	5	Data Out
Standby	H	X	5	5	High Z
Program	Pulsed L to H	H	25	5	Data In
Program Verify	L	L	25	5	Data Out
Program Inhibit	H	H	25	5	High Z

1/ Positive Logic: H = High logic level
L = Low logic level
X = Irrelevant
HI-Z = High-impedance state

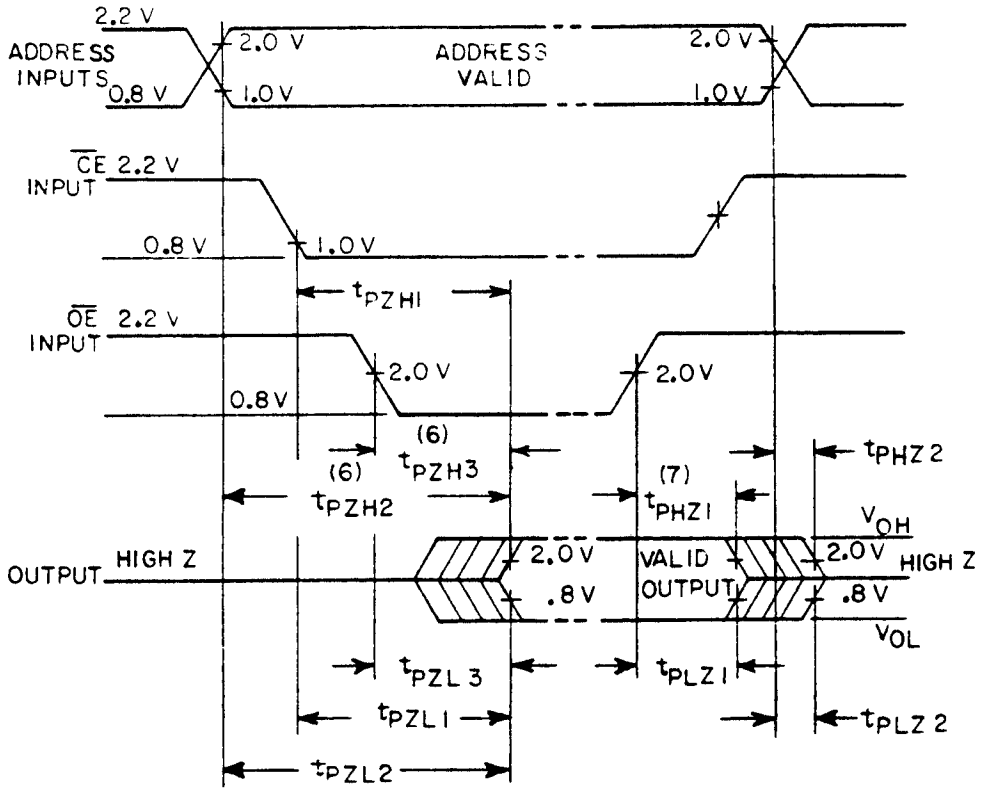
2/ Outputs have internal active pull-ups.

FIGURE 2. Truth table.



NOTES:
1. A_0 = least significant address bit; A_{10} = most significant address bit.
2. O_0 = least significant data output bit; O_7 = most significant data output bit.

FIGURE 3. Functional block diagram.



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. C_L = 100 pF includes jig and probe capacitance. Z_1 = TTL gate or equivalent.

FIGURE 4. Propagation delay time test circuit and waveforms.

NOTES: (Continued)
3. Input rise and fall times $\leq$ 20 ns.
4. Input pulse levels 0.8 V to 2.2 V.
5. Timing measurement reference levels: Inputs 1.0 V and 2.0 V, outputs 0.8 V and 2.0 V.
6. $\overline{OE}$ may be delayed up to (t_{PZH2} or t_{PZL2}) - (t_{PZH3} or t_{PZL3}) after the falling edge of $\overline{CE}$ without impact on t_{PZH2} or t_{PZL2}.
7. t_{PZH3} or t_{PZL3} is specified from $\overline{OE}$, whichever comes first.

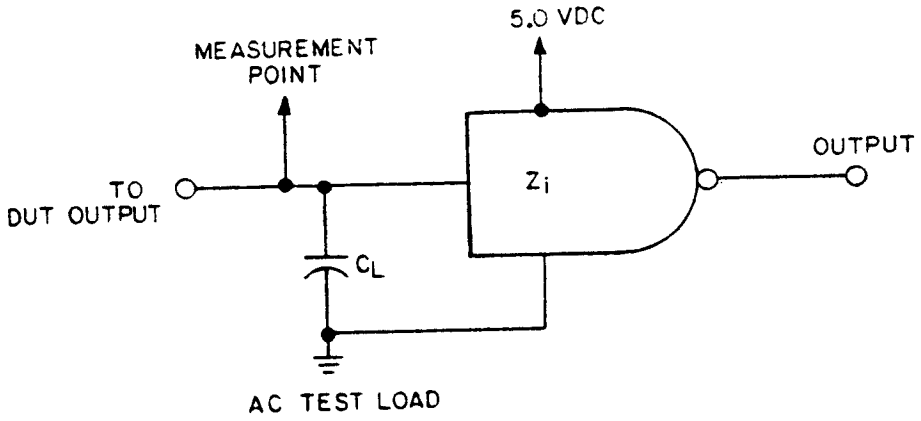
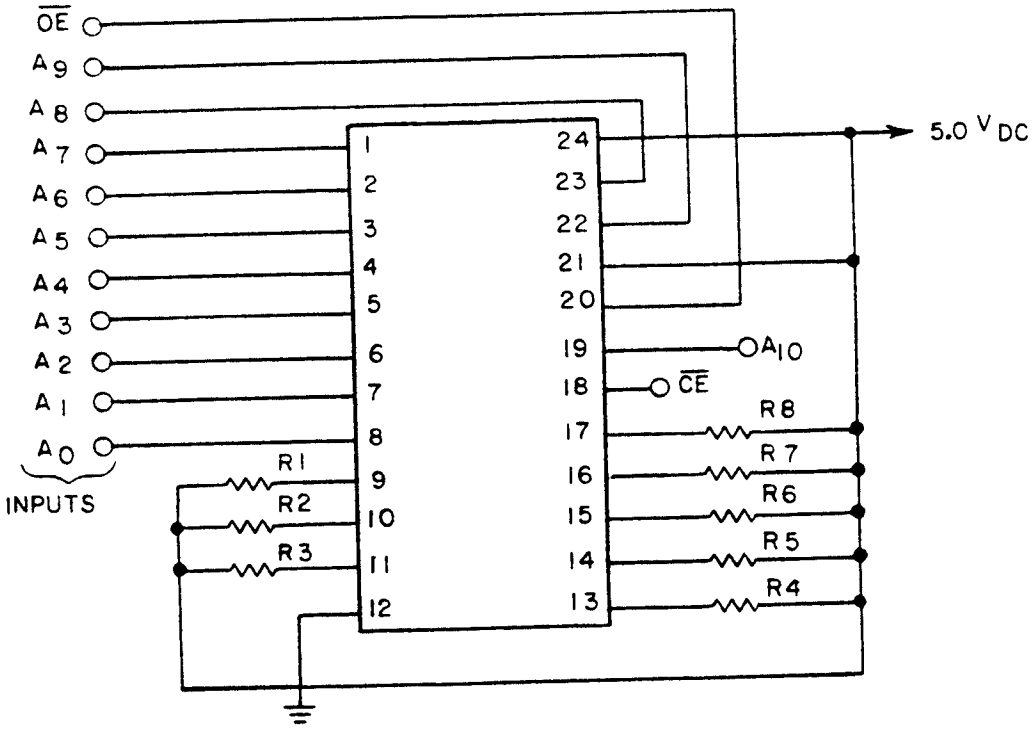


FIGURE 4. Propagation delay time test circuit and waveforms - Continued.



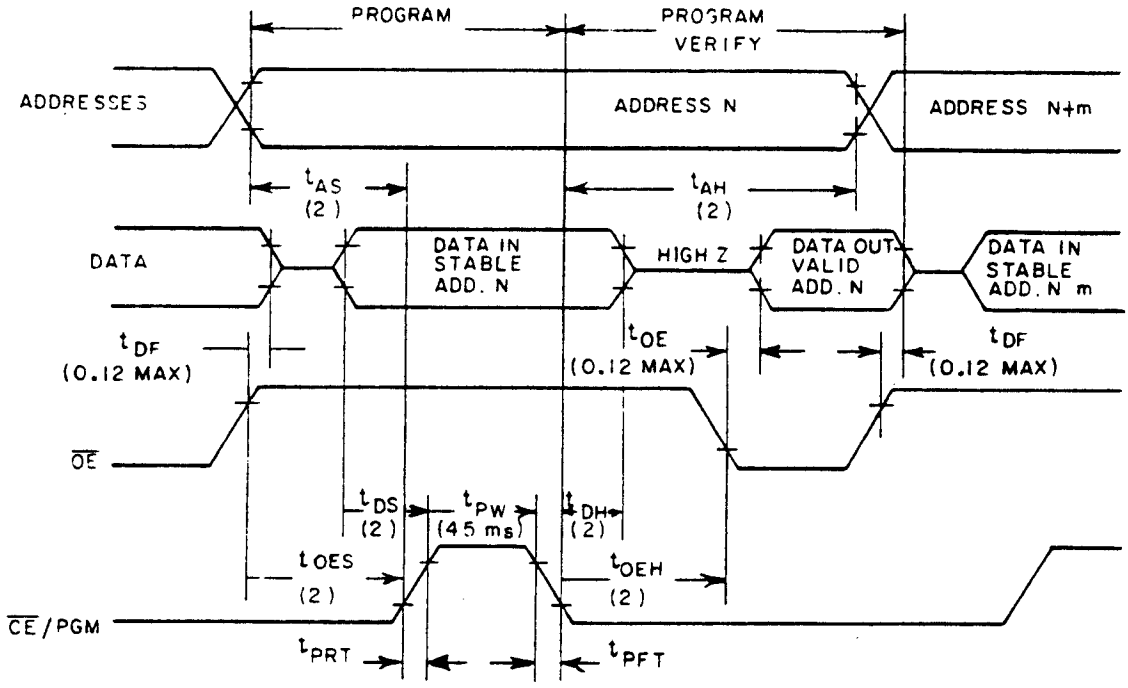
NOTES:

1. R1 thru R8 = 3.6 kΩ ±5.0% when CE input is pulsed:
   = 1.0 kΩ ±5.0% when CE is at $V_{IH} \geq 2.4$ V.
2. Input signal characteristics: Amplitude: $V_{IH} \geq 2.4$ V, $V_{IL} \leq 0.4$ V; Duty cycle = 50%, $t_{THL} \leq 100$ ns and the following PRR (±20%).

Input	PRR	Input	PRR
A_0	16 kHz $\leq f_0 \leq$ 100 kHz	A_7	$f_0 \div 128$
A_1	$f_0 \div 2$	A_8	$f_0 \div 256$
A_2	$f_0 \div 4$	A_9	$f_0 \div 512$
A_3	$f_0 \div 8$	A_{10}	$f_0 \div 1024$
A_4	$f_0 \div 16$	$\overline{CE}$	$f_0 \div 2048$ (Pulse mode)
A_5	$f_0 \div 32$	or $\overline{CE}$	= V_{IH} (De-select mode)
A_6	$f_0 \div 64$		

3. Device under test may be operated with $\overline{CE}$ input pulsed or at V_{IH}.

FIGURE 5. Burn-in and steady state life test circuit.



NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% to 90%) are 20 ns.
4. Input pulse levels are 0.8 V to 2.2 V.
5. All times shown in parentheses are minimum times in µs unless other specified.

FIGURE 6. Programming waveforms.

TABLE III. Group A inspection for device type 01.

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits Min	Test limits Max	Test limits Unit
1	V_{OH}	3006	1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	GND	O_3	O_4	O_5	O_6	O_7	$\overline{CE}$	A_{10}	$\overline{OE}$	V_{PP}	A_9	A_8	V_{CC}	O_0	2.4		
T_C = +25°C			2	1/	1/	1/	1/	1/	1/	1/	1/	-400 µA	-400 µA								0.8 V	1/	0.8 V	4.5 V	1/	1/	4.5 V	O_1			
			3											-400 µA														O_2			
			4													-400 µA												O_3			
			5														-400 µA											O_4			
			6															-400 µA										O_5			
			7																-400 µA									O_6			
			8																	-400 µA								O_7			
	V_{OL}	3007	9									2.1 mA												5.5 V			5.5 V	O_0		0.45	
			10										2.1 mA															O_1			
			11											2.1 mA														O_2			
			12													2.1 mA												O_3			
			13														2.1 mA											O_4			
			14															2.1 mA										O_5			
			15																2.1 mA									O_6			
			16																	2.1 mA								O_7			
	I_{LO} 2/		17	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V									2.4 V	2.4 V			2.4 V	2.4 V		O_0		10	µA
			18										5.5 V															O_1			
			19											5.5 V														O_2			
			20													5.5 V												O_3			
			21														5.5V											O_4			
			22															5.5 V										O_5			
			23																5.5 V									O_6			
			24																	5.5 V								O_7			
	I_{IH}	3010	25	5.5 V																								A_7			
			26		5.5 V																							A_6			
			27			5.5 V																						A_5			
			28				5.5 V																					A_4			
			29					5.5 V																				A_3			

TABLE III. Group A inspection for device type 01 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas terminal	Test limits Min	Test limits Max	Test limits Unit
1	I_{IH}	3010	30						5.5 V						GND								0.8 V	5.5 V			5.5 V	A_2		10	µA
T_C = +25°C			31							5.5 V																		A_1			
			32								5.5 V																	A_0			
			33																			5.5 V						A_{10}			
			34																						5.5 V			A_9			
			35																							5.5 V		A_8			
			36																		5.5 V							$\overline{CE}$			
	I_{IL}		37	0.8 V																								A_7			
			38		0.8 V																							A_6			
			39			0.8 V																						A_5			
			40				0.8 V																					A_4			
			41					0.8 V																				A_3			
			42						0.8 V																			A_2			
			43							0.8 V																		A_1			
			44								0.8 V																	A_0			
			45																			0.8 V						A_{10}			
			46																						0.8 V			A_9			
			47																							0.8 V		A_8			
			48																		0.8 V							$\overline{CE}$			
	I_{SB}	3005	49	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	2.4 V				2.4 V	2.4 V		V_{CC}		30	mA
	I_{CC}	3005	50	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	0.8 V			5.5 V	2.4 V	2.4 V		V_{CC}		115	mA
	I_{PP}	3005	51	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	2.4 V	1/	0.8 V	6.10 V	2.4 V	2.4 V	5.5 V	V_{PP}		4	mA
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125°C.																														
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55°C.																														
7 T_C = +25°C	Functional tests	3014	52	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	1/ All outputs			
8	Same tests, terminal conditions and limits as for subgroup 7, except T_C = +125°C and -55°C.																														
9	t_{PZH1}		53	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	GND	6/	7/	7/	6/	6/	7/	Outputs		7/	ns
T_C = +25°C	t_{PZL1}		54	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	GND	6/	7/	7/	6/	6/	7/	Outputs		7/	ns

TABLE III. Group A inspection for device type 01 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test limits Min	Max	Unit
				A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	GND	O_3	O_4	O_5	O_6	O_7	$\overline{CE}$	A_{10}	$\overline{OE}$	V_{PP}	A_9	A_8	V_{CC}				
9	t_{PZH2}		55	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	GND	6/	7/	7/	6/	6/	7/	Outputs		7/	ns
T_C = +25°C	t_{PZL2}		56																												
	t_{PZH3}		57																												
	t_{PZL3}		58																												
	t_{PHZ1}		59																												
	t_{PLZ1}		60																												
	t_{PHZ2}		61																												
	t_{PLZ2}		62																												
10	Same tests, terminal conditions and limits as for subgroup 9, except T_C = +125°C.																														
11	Same tests, terminal conditions and limits as for subgroup 9, except T_C = -55°C.																														

1/ Before performing electrical tests, a binary count pattern shall be programmed into the devices submitted for acceptance. V_{IH} (2.4 V) or V_{IL} = 0.8 V shall be applied to the applicable address pins to set the measured terminal in the proper state for measurement.

2/ Connect all address inputs and the $\overline{CE}$ input to V_{IH} and measure I_{LO} with the output under test connected to the voltages specified.

3/ Output pins (O1 thru O6) shall be open.

4/ I_{PP} = 5 mA @ 25°C and 125°C.
I_{PP} = 10 mA @ -55°C.

5/ Tests shall verify binary count pattern. All bits shall be tested with the following conditions:
a. V_{CC} = 5.5 V
b. V_{CC} = 4.5 V
c. Inputs: H = 2.0 V and L = 0.8 V.
d. Outputs: Output voltage shall be either.
1. H = 2.4 V minimum and L = 0.8 V maximum when using a high speed checker double comparator.
2. H $\geq$ 1.0 V and L $\leq$ 1.0 V when using a high speed checker single comparator.

6/ Each output shall be connected to the load circuit shown on figure 4 and propagation delay times shall be measured as follows:
a. $\overline{CE}$ input to programmed ouputs. Condition address inputs A_0 thru A_{10} to set outputs under test to the "L" state.
Pulse $\overline{CE}$ input and measure t_{PLZ} and t_{PZL}.
b. Address inputs to outputs. Pulse $\overline{CE}$ input. Measure t_{PLH} and t_{PHL} from each address input to each output. Output under test shall be alternately changed from its low level to its high level by addressing the appropriate word combinations.

7/ See table I herein for supply voltages and test limits.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows.

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified. Where use of electrical rejects is permitted, no programming is required.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the reference terminal.

4.6 Programming procedures. The following procedures shall be followed when programming and verification testing is performed. The waveforms and timing relationships shown on figure 6 and the test conditions and limits specified in table IV shall be adhered to.

a. Initially, and after each erasure, all bits are in the "H" state (output high). Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure.

b. The circuit is set up for programming operating by $\overline{OE}$/PGM input to V_{OH} and Vpp set to 25 ±1.0 V. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-bits in parallel, are presented to the data lines (O_0-O_7). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). The programming time for a single bit is only 50 ms and for all bits is approximately 100 seconds.

c. A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with Vpp at 25 V. $\overline{OE}$ and $\overline{CE}$/PGM must be at V_{OL}.

4.7 Erasing procedure. The device is erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short-wave ultraviolet lamp. The lamp should be used without short-wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

4.8 High-voltage (V_{ZAP}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 150 volts from a 100-picofarad source in the following test sequence:

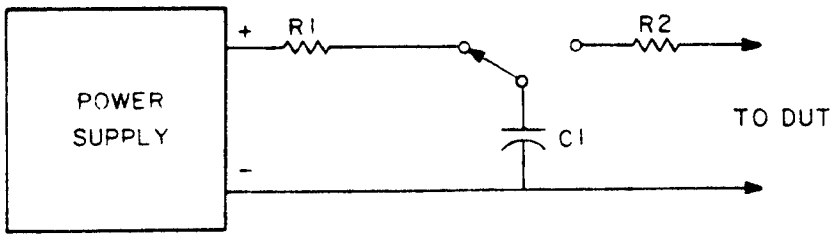
a. Measure I_{IH} and I_{IL} at one input terminal of the DUT at +25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal of I_{IH} and I_{IL} shall be ±10 µA, maximum.

b. In the circuit below, charge the capacitor to -150 V. Then, using the same terminal of the device as selected above for leakage measurements, switch the capacitor to discharge into the device terminal. Then repeat the procedure with +150 V (see figure 7).

c. Within 24 hours, repeat the measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

TABLE IV. Programming characteristics.

Parameter	Symbol	Test conditions	Limits Min	Limits Max	Unit
V_{CC} supply current	I_{CC}	T_C = +25°C, V_{CC} = 5.0 V, V_{IH} = 2.0 V min, V_{IL} = 0.80 max, V_{IH} = ($\overline{CS}$) = 5.0 V, ±10%		100	mA
V_{PP} supply current	I_{PP1}	V_{PP} = 5.5 V, $\overline{CE}$/PGM = V_{IL}		5	mA
Program pulse current	I_{PP2}	$\overline{CE}$/PGM = V_{IH}, V_{PP} = 25 V ±1.0 V		30	mA
Address setup time	t_{AS}	See figure 6 and 4.6.	2		ns
$\overline{OE}$ setup time	t_{OES}		2		ns
Data setup time	t_{DS}		2		ns
Address hold time	t_{AH}		2		ns
$\overline{OE}$ hold time	t_{OEH}		2		ns
Data hold time	t_{DH}		2		ns
Chip deselect to output float delay	t_{DF}	See 4.6	0	120	ns
Output enable to output delay	t_{OE}	See figure 6 and 4.6.		120	ns
Program pulse width	t_{PW}		45	55	ns
Program pulse rise time	t_{PRT}		5	100	ns
Program pulse fall time	t_{PFT}		5	100	ns



NOTE: R1 = Appropriate current-limiting resistance.
R2 = 1.5 kΩ ±5%.
C1 = 100 pF ±20%.
Power supply voltage = V_{ZAP} = +150 Vdc and -150 Vdc.

FIGURE 7. High voltage (V_{ZAP}) test.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logisitic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5005 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

t_{pyx} - - - - - - - - - - - - - - - Output invalid address change.
V_{IN} - - - - - - - - - - - - - - - Voltage level at an input terminal.
I_{IN} - - - - - - - - - - - - - - - Current flowing into an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation to static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Device should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS area.

f. Maintain relative humidity above 50 percent, if practical.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of the MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the packaged represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	2716

6.10 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

Agent:
DLA - ES

Preparing activity:
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